

EXAMINER'S AMENDMENT

1. Claims 1, 3, and 4 are pending in the instant application. Claims 5-12 are withdrawn.
2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Shawn B. Cage on September 12, 2008.

The application has been amended as follows wherein the following versions of claims 1 and 3 replace all prior versions in their entirety and claims 4 and 5-12 are CANCELLED:

1. A clock data recovery circuit comprising:
 - a voltage control oscillator that generates a clock;
 - a data identifier that identifies input data based on the clock generated by the voltage control oscillator;
 - a frequency divider that divides a frequency of the input data;
 - a duty ratio detector that determines a duty ratio of the input data;
 - a variable delaying unit that generates a delay clock, which is obtained by delaying the clock generated by the voltage control oscillator based on a the duty ratio of the input data; and

a phase comparator that detects a phase difference between a phase of the delay clock generated by the variable delaying unit and a phase of the input data of which frequency is divided by the frequency divider, and generates a phase difference signal to eliminate the detected phase difference,

wherein the voltage control oscillator generates the clock by adjusting an oscillation frequency based on the phase difference signal, and outputs the clock to both the data identifier and the ~~phase comparator~~ variable delaying unit.

3. The clock data recovery circuit according to claim 1,

wherein ~~the~~ a predetermined time to be used to delay the clock generated by the voltage control oscillator to generate the delay clock is set based on the duty ratio of the input data.

4. (Cancelled) ~~The clock data recovery circuit according to claim 1, further comprising:~~

~~a duty ratio detector that determines a delay time to be used to delay the clock generated by the voltage control oscillator based on the duty ratio of the input data, and outputs the determined delay time to the variable delaying unit.~~

Claims 5-12. (Cancelled)

Claims 1 and 3 are renumbered respectively as claims 1 and 2.

Allowable Subject Matter

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3. Claims 1 and 3 renumbered respectively as claims 1 and 2 are allowed.
4. The following is an examiner's statement of reasons for allowance:

Claims 1 and 3 renumbered respectively as claims 1 and 2 are allowed because the prior art of record does not disclose every claimed feature. As noted in the Applicant's remarks filed July 21, 2008, the duty ratio detector of Ishihara is applied particularly to a sample and hold circuitry for a specific implementation. The application of Ishihara's duty ratio detector to a variable delaying unit (such as in the combination of Vallet in view of Gossmann) is not an obvious modification for the reasons outlined in Applicant's response of July 21, 2008.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Art Unit 2611
September 12, 2008

/jmp/

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611